



PSMN5R0-30YL

N-channel 30 V 5 mΩ logic level MOSFET in LPAK

Rev. 4 — 9 March 2011

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in industrial and communications applications.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive sources

1.3 Applications

- Class-D amplifiers
- DC-to-DC converters
- Motor control
- Server power supplies

1.4 Quick reference data

Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|----------------------------------|---|-----|------|-----|------|
| V_{DS} | drain-source voltage | $T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$ | - | - | 30 | V |
| I_D | drain current | $T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see Figure 1 | - | - | 91 | A |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ °C};$ see Figure 2 | - | - | 61 | W |
| T_j | junction temperature | | -55 | - | 175 | °C |
| Static characteristics | | | | | | |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = 10\text{ V}; I_D = 15\text{ A};$ $T_j = 25\text{ °C}$ | - | 3.63 | 5 | mΩ |
| Dynamic characteristics | | | | | | |
| Q_{GD} | gate-drain charge | $V_{GS} = 4.5\text{ V}; I_D = 10\text{ A};$ $V_{DS} = 12\text{ V};$ see Figure 14 ; see Figure 15 | - | 3.8 | - | nC |

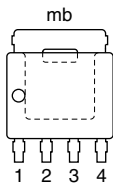
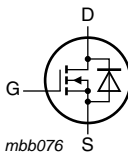


Table 1. Quick reference data ...continued

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------------|--|--|-----|------|-----|------|
| $Q_{G(\text{tot})}$ | total gate charge | $V_{GS} = 4.5 \text{ V}$; $I_D = 10 \text{ A}$; $V_{DS} = 12 \text{ V}$; see Figure 14 | - | 14.1 | - | nC |
| Avalanche ruggedness | | | | | | |
| $E_{DS(\text{AL})S}$ | non-repetitive drain-source avalanche energy | $V_{GS} = 10 \text{ V}$; $T_{j(\text{init})} = 25 \text{ }^\circ\text{C}$; $I_D = 84 \text{ A}$; $V_{\text{sup}} \leq 30 \text{ V}$; $R_{GS} = 50 \text{ } \Omega$; unclamped | - | - | 32 | mJ |

2. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-----------------------------------|--|---|
| 1 | S | source |  |  |
| 2 | S | source | | |
| 3 | S | source | | |
| 4 | G | gate | | |
| mb | D | mounting base; connected to drain | | |

SOT669 (LFPAK)

3. Ordering information

Table 3. Ordering information

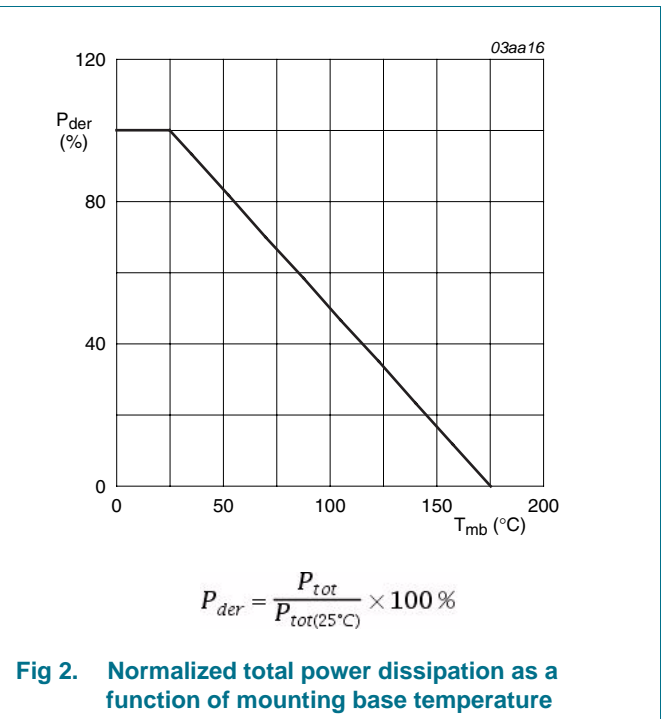
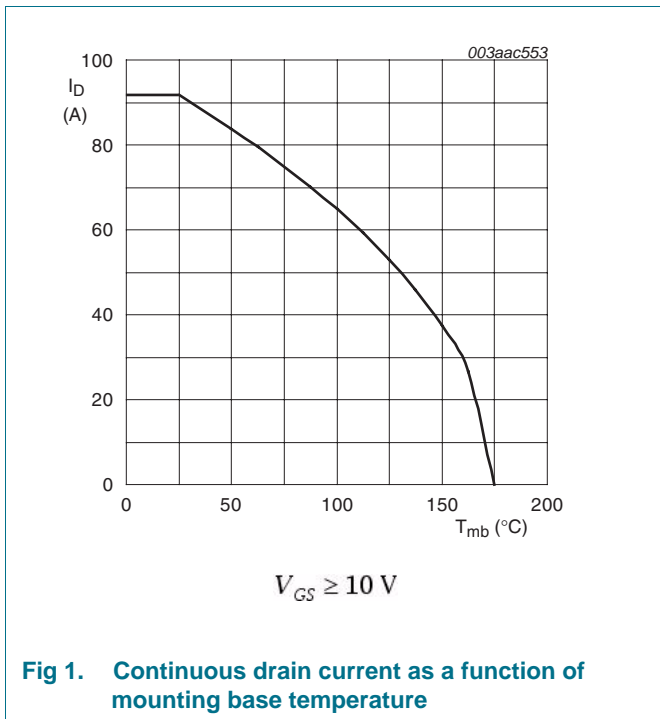
| Type number | Package | | Version |
|--------------|---------|---|---------|
| | Name | Description | |
| PSMN5R0-30YL | LFPAK | plastic single-ended surface-mounted package (LFPAK); 4 leads | SOT669 |

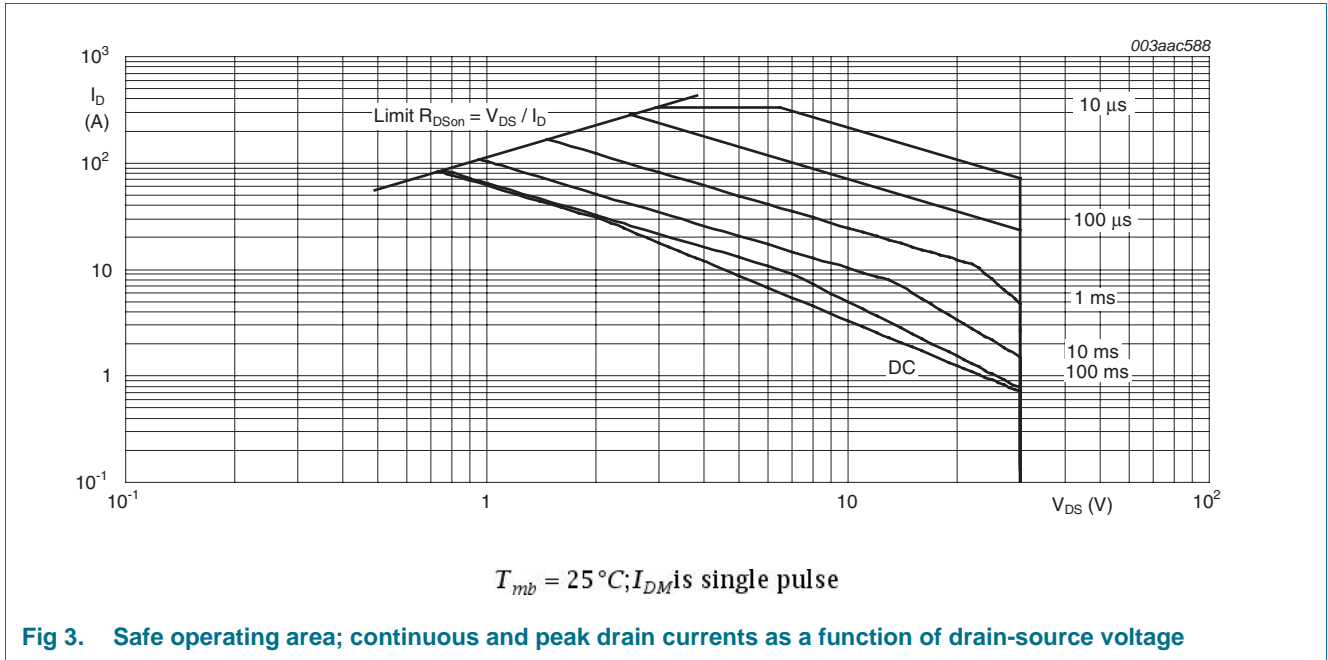
4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------------------------|--|---|-----|-----|------|
| V_{DS} | drain-source voltage | $T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$ | - | 30 | V |
| V_{DSM} | peak drain-source voltage | $t_p \leq 25\text{ ns}; f \leq 500\text{ kHz}; E_{DS(AL)} \leq 130\text{ nJ}; \text{pulsed}$ | - | 35 | V |
| V_{DGR} | drain-gate voltage | $T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}; R_{GS} = 20\text{ k}\Omega$ | - | 30 | V |
| V_{GS} | gate-source voltage | | -20 | 20 | V |
| I_D | drain current | $V_{GS} = 10\text{ V}; T_{mb} = 100\text{ °C}; \text{see Figure 1}$ | - | 64 | A |
| | | $V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}; \text{see Figure 1}$ | - | 91 | A |
| I_{DM} | peak drain current | pulsed; $t_p \leq 10\text{ }\mu\text{s}; T_{mb} = 25\text{ °C}; \text{see Figure 3}$ | - | 336 | A |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ °C}; \text{see Figure 2}$ | - | 61 | W |
| T_{stg} | storage temperature | | -55 | 175 | °C |
| T_j | junction temperature | | -55 | 175 | °C |
| Source-drain diode | | | | | |
| I_S | source current | $T_{mb} = 25\text{ °C}$ | - | 84 | A |
| I_{SM} | peak source current | pulsed; $t_p \leq 10\text{ }\mu\text{s}; T_{mb} = 25\text{ °C}$ | - | 336 | A |
| Avalanche ruggedness | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $V_{GS} = 10\text{ V}; T_{j(\text{init})} = 25\text{ °C}; I_D = 84\text{ A}; V_{sup} \leq 30\text{ V}; R_{GS} = 50\text{ }\Omega; \text{unclamped}$ | - | 32 | mJ |

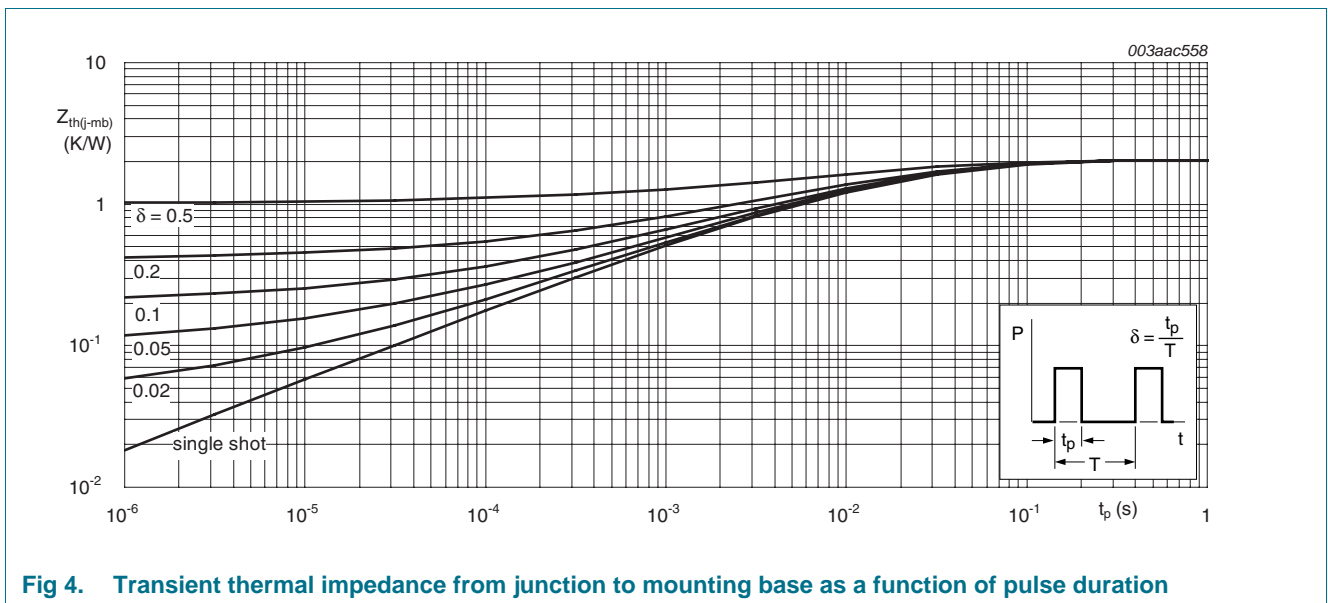




5. Thermal characteristics

Table 5. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|---|------------------------------|-----|------|-----|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | see Figure 4 | - | 1.39 | 2 | K/W |



6. Characteristics

Table 6. Characteristics
Tested to JEDEC standards where applicable.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|-----------------------------------|--|------|------|------|---------------|
| Static characteristics | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | 30 | - | - | V |
| | | $I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$ | 27 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 11 ; see Figure 12 | 1.3 | 1.7 | 2.15 | V |
| | | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ\text{C};$ see Figure 12 | 0.65 | - | - | V |
| | | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see Figure 12 | - | - | 2.45 | V |
| I_{DSS} | drain leakage current | $V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | - | - | 1 | μA |
| | | $V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$ | - | - | 100 | μA |
| I_{GSS} | gate leakage current | $V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | - | - | 100 | nA |
| | | $V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | - | - | 100 | nA |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = 4.5 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$ | - | 5.08 | 6.7 | mΩ |
| | | $V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 150 \text{ }^\circ\text{C};$ see Figure 13 | - | - | 8.7 | mΩ |
| | | $V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$ | - | 3.63 | 5 | mΩ |
| R_G | gate resistance | $f = 1 \text{ MHz}$ | - | 0.69 | 1.5 | Ω |
| Dynamic characteristics | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D = 10 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 4.5 \text{ V};$ see Figure 14 | - | 14.1 | - | nC |
| | | $I_D = 10 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 14 ; see Figure 15 | - | 29 | - | nC |
| | | $I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$ | - | 27 | - | nC |
| Q_{GS} | gate-source charge | $I_D = 10 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 4.5 \text{ V};$ see Figure 14 ; see Figure 15 | - | 4.3 | - | nC |
| $Q_{GS(th)}$ | pre-threshold gate-source charge | | - | 2.9 | - | nC |
| $Q_{GS(th-pl)}$ | post-threshold gate-source charge | | - | 1.4 | - | nC |
| Q_{GD} | gate-drain charge | | - | 3.8 | - | nC |
| $V_{GS(pl)}$ | gate-source plateau voltage | $V_{DS} = 12 \text{ V};$ see Figure 14 ; see Figure 15 | - | 2.5 | - | V |
| C_{iss} | input capacitance | $V_{DS} = 12 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see Figure 16 | - | 1760 | - | pF |
| C_{oss} | output capacitance | | - | 373 | - | pF |
| C_{rss} | reverse transfer capacitance | | - | 171 | - | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS} = 12 \text{ V}; R_L = 0.5 \text{ } \Omega; V_{GS} = 4.5 \text{ V};$ $R_{G(ext)} = 4.7 \text{ } \Omega$ | - | 19 | - | ns |
| t_r | rise time | | - | 35 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 29 | - | ns |
| t_f | fall time | | - | 12 | - | ns |

Table 6. Characteristics ...continued
 Tested to JEDEC standards where applicable.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------------|-----------------------|--|-----|------|-----|------|
| Source-drain diode | | | | | | |
| V_{SD} | source-drain voltage | $I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$; see Figure 17 | - | 0.84 | 1.2 | V |
| t_{rr} | reverse recovery time | $I_S = 20\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; | - | 30 | - | ns |
| Q_r | recovered charge | $V_{DS} = 20\text{ V}$ | - | 21 | - | nC |

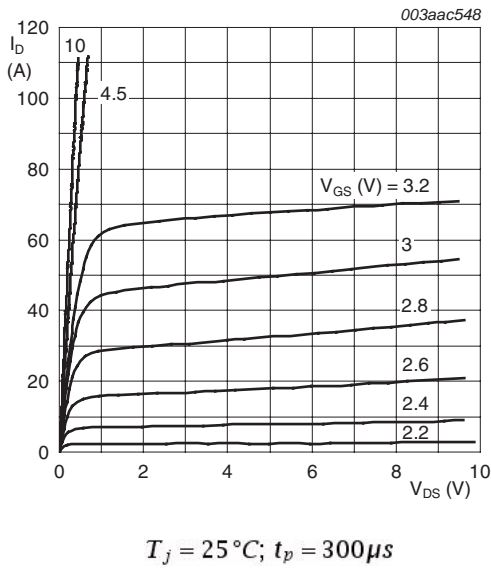


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

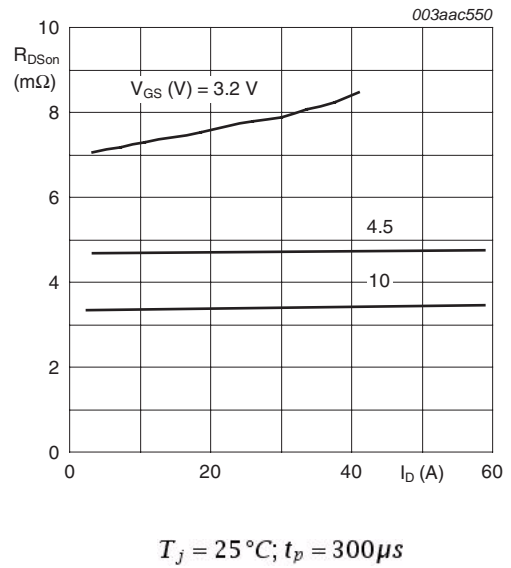


Fig 6. Drain-source on-state resistance as a function of drain current; typical values

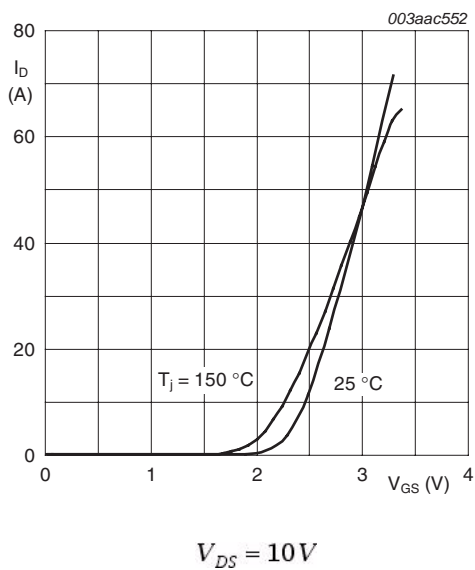


Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values

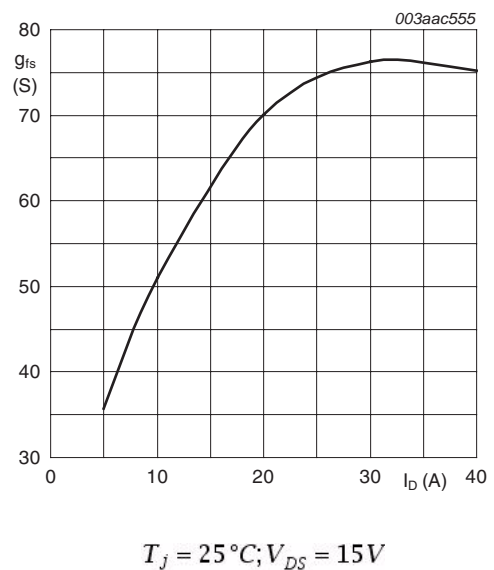
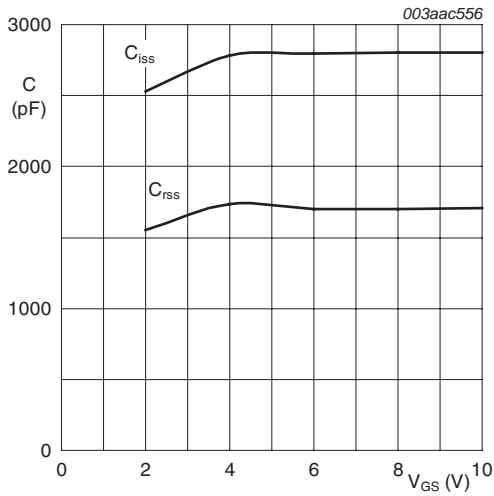
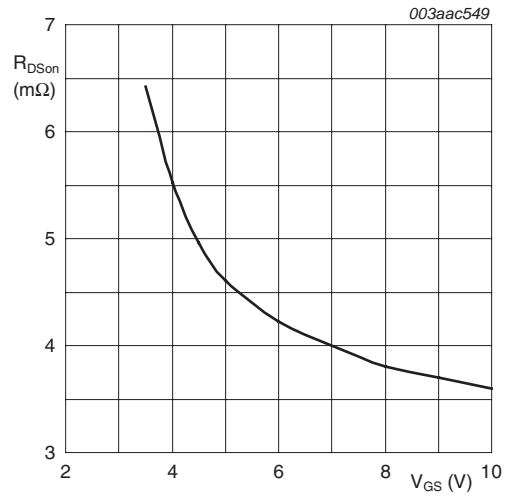


Fig 8. Forward transconductance as a function of drain current; typical values



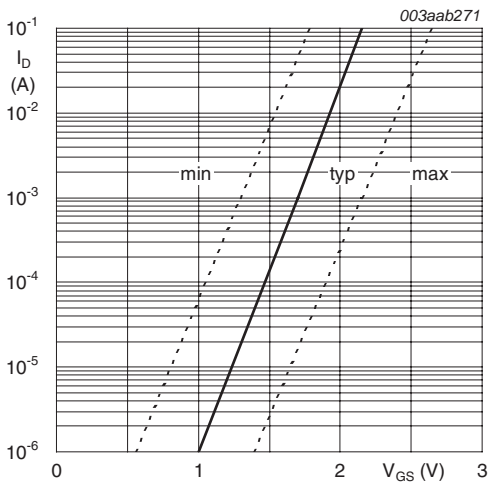
$V_{DS} = 0V; f = 1MHz$

Fig 9. Input and reverse transfer capacitances as a function of gate-source voltage; typical values



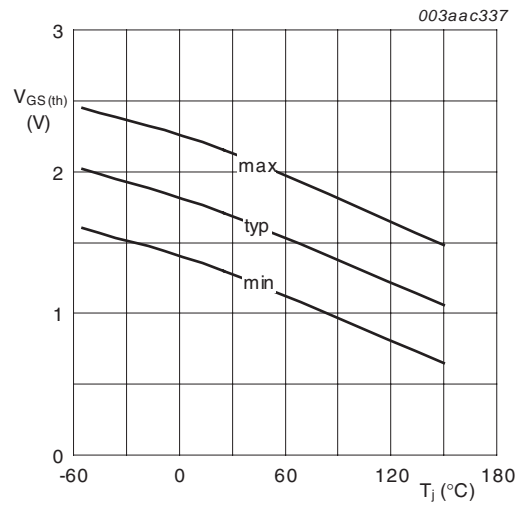
$T_j = 25^\circ C; I_D = 15A$

Fig 10. Drain-source on-state resistance as a function of gate-source voltage; typical values



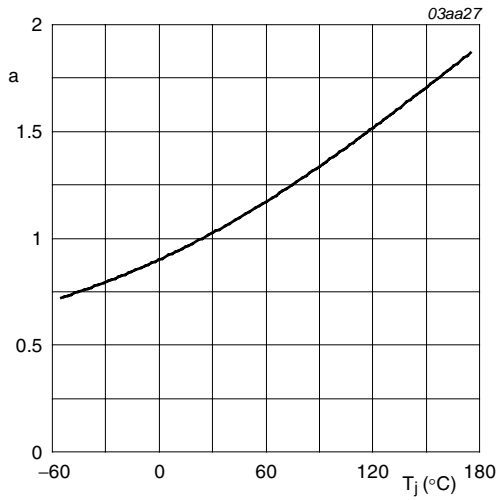
$T_j = 25^\circ C; V_{DS} = 5V$

Fig 11. Sub-threshold drain current as a function of gate-source voltage



$I_D = 1mA; V_{DS} = V_{GS}$

Fig 12. Gate-source threshold voltage as a function of junction temperature



$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ\text{C})}}$$

Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature

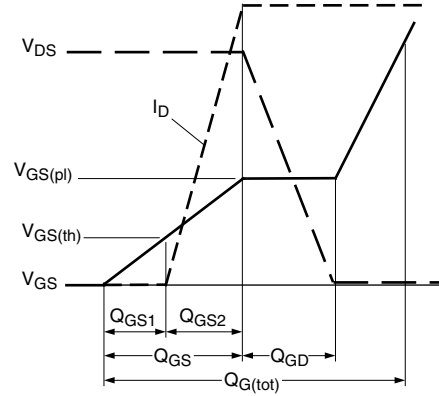
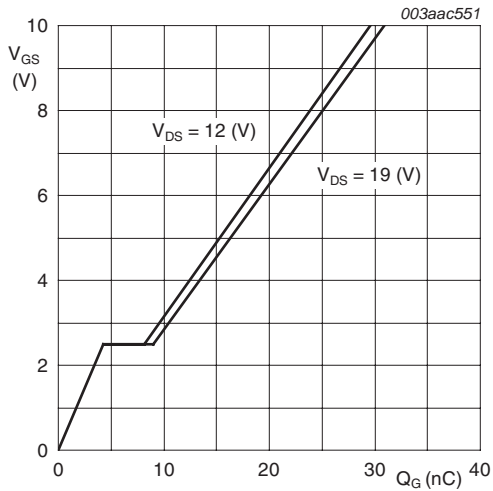
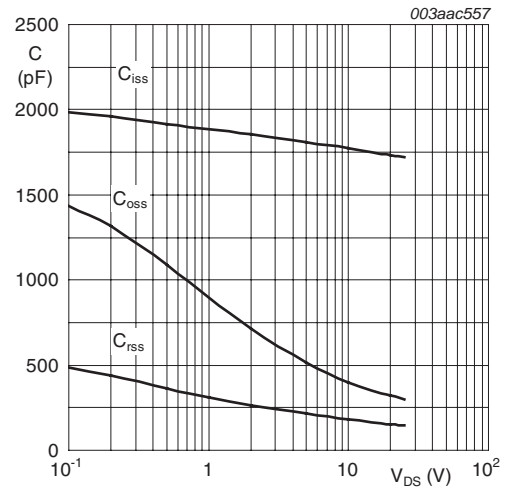


Fig 14. Gate charge waveform definitions



$$T_j = 25^\circ\text{C}; I_D = 10\text{A}$$

Fig 15. Gate-source voltage as a function of gate charge; typical values



$$V_{GS} = 0\text{V}; f = 1\text{MHz}$$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

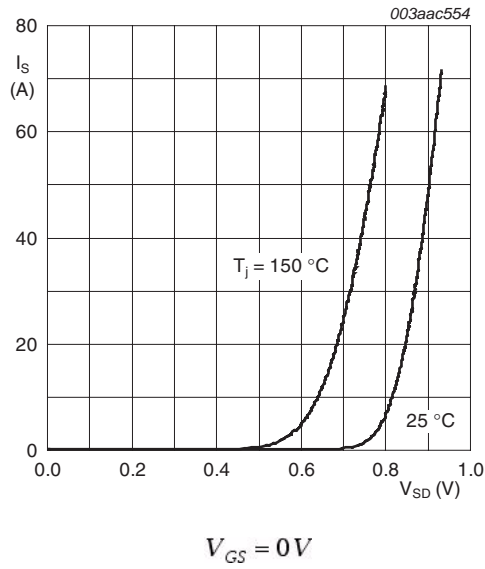


Fig 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (LPAK); 4 leads

SOT669

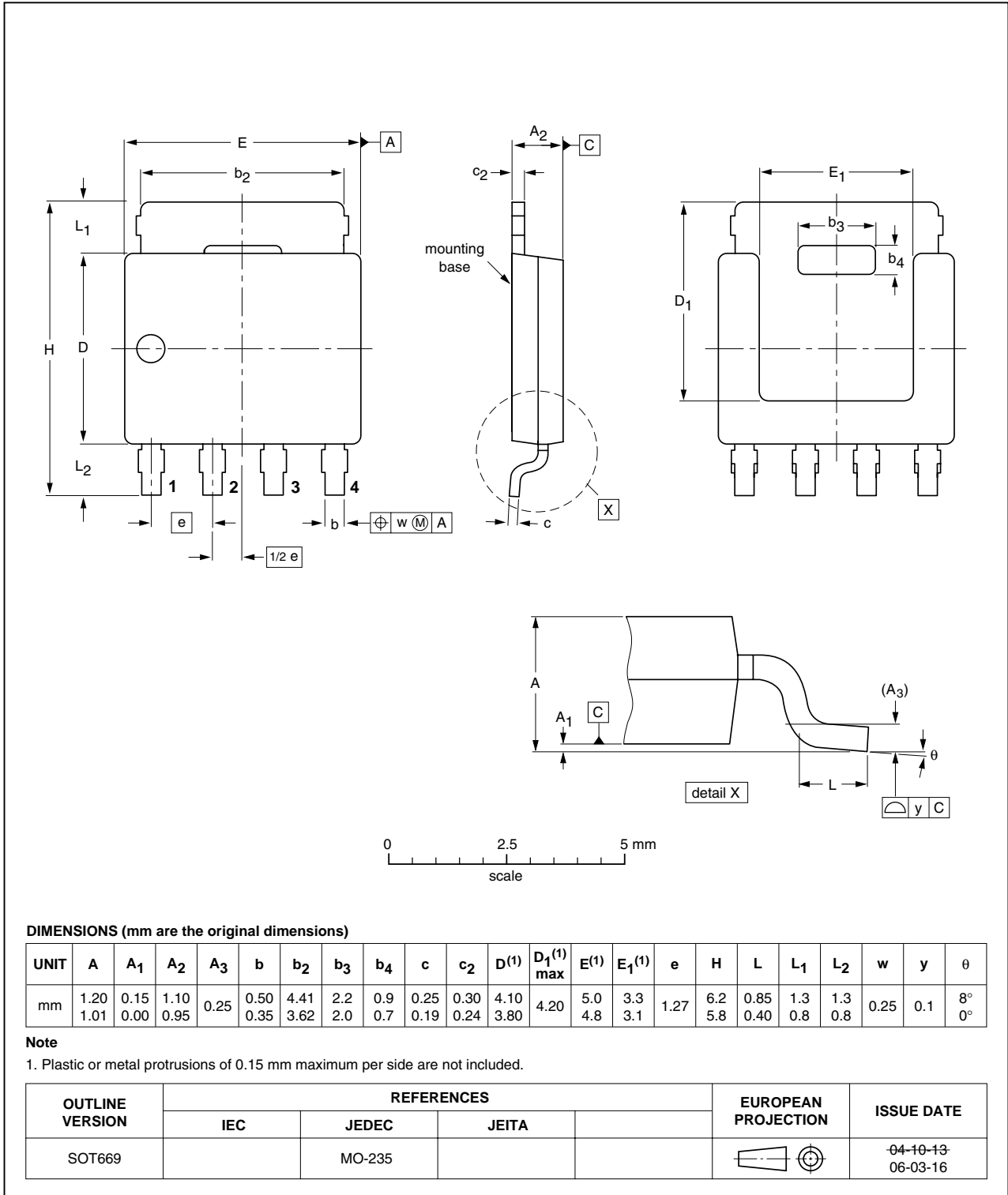


Fig 18. Package outline SOT669 (LPAK)

8. Revision history

Table 7. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|------------------|-------------------------------|--------------------|---------------|----------------|
| PSMN5R0-30YL v.4 | 20110309 | Product data sheet | - | PSMN5R0-30YL_3 |
| Modifications: | • Various changes to content. | | | |
| PSMN5R0-30YL_3 | 20100104 | Product data sheet | - | PSMN5R0-30YL_2 |

9. Legal information

9.1 Data sheet status

| Document status ^[1] ^[2] | Product status ^[3] | Definition |
|---|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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